IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF APPEALS

In re Patent Application of: BEAUJOIN ET AL.	)	
Serial No. 10/075,113	)	Examiner: J. TABONE, JR
Confirmation No: 6957	)	Art Unit: 2133
Filing Date: FEBRUARY 13, 2002	)	
For: METHOD OF TESTING A SEQUENTIAL ACCESS MEMORY PLANE AND A CORRESPONDING SEQUENTIAL ACCESS MEMORY SEMICONDUCTOR DEVICE	)	

APPELLANTS' SUMMARY OF THE CLAIMED SUBJECT MATTER UNDER 37 C.F.R. 41.37(c)(1)(v)

MS Appeal Brief-Patents
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Sir:

Submitted is Appellants' Summary of the Claimed Subject Matter in response to the Notice of Non-Compliant Appeal Brief mailed November 28, 2007. The PTO Notice alleged that the brief filed June 26, 2007 was deficient, and that a paper providing a new Summary of the Claimed Subject Matter is required. If any additional extension and/or fee is required, authorization is given to charge Deposit Account No. 01-0484.

A. Summary of the Claimed Subject Matter

In general, the invention is directed to testing a sequential access memory array with a straightforward implementation leading to a reduced overall size of the test logic. Referring to FIG. 1 (reproduced below) and page 5, line 12 through page 8, line 19 of the specification, for example, the presently claimed invention will now be described.

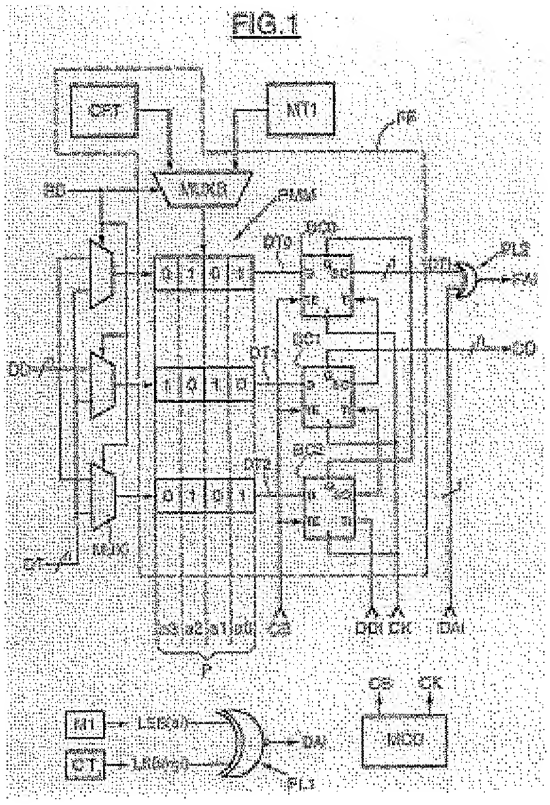

FIG. 1 of the Present Application.

Figure 1 shows a sequential access memory device FF, for example, a FIFO memory. The memory FF includes a memory array PMM able to store p words each of n bits. In other words, the depth of the memory is equal to p and the width of the data bus is equal to n. In the example described here, for simplicity, p = 4 and n = 3. The figure shows the successive storage addresses ai of the p words in the memory array PMM.

In the normal operating mode writing and reading are effected in the conventional manner using write and read pointers controlled in the conventional manner by control circuit/means CPT. A multiplexer MUXB controls the write and read pointers of the memory array in response to a control

signal RB from either the control means CPT (in the normal mode of operation) or the test mode control circuit/means MT1 (in the test mode of operation). Similarly, the data to be written into the memory array is selected via n multiplexers MUXi which are also controlled by the control signal RB.

Accordingly, in the normal mode of operation, the n data bits DD on the bus are written into the memory array. In the test mode of operation, on the other hand, binary test data bits DT are written into the memory plane PMM.

The control means or control circuit MT1 and the multiplexers MUXi and MUXB then form first test circuit or means used, in conjunction with the test data bits DT, to write into the memory array p test words each made up of n test bits. Also, in a preferred embodiment, the first test means write the p test words of n bits in such a way as to obtain a checkerboard test configuration in the memory plane. A checkerboard configuration, as shown in Figure 1, is one in which each test word includes alternating 0 and 1 bits, and wherein the 0 bits and the 1 bits of two words written at successive addresses are mutually shifted by one bit.

The memory FF further includes n output registers BC0-BC2. Here the output registers are D-type flip-flops each having a data input D connected to one of the n outputs of the memory plane PMM. Each flip-flop D also has a test input TI, a test output SO and a test control input TE. Furthermore, each flip-flop is clocked by a clock signal CK. Finally, each flip-flop has a data output Q.

In the normal mode of operation the n data bits extracted from the memory PMM are delivered to the respective n data inputs D of the flip-flops and then to the n data outputs Q in time with the rising edges of the clock signal CK. This is not the case in the test mode of operation, however, as explained next in more detail.

As well as being connected to n respective outputs of the memory plane PMM by their data input D, the n flip-flops are chained. To be more precise, the test output SO of one flip-flop, for example the flip-flop BC1, is connected to the test input TI of the adjacent flip-flop, here the flip-flop BC0, for example, to form a chain. The test input TI of the first flip-flop BC2 in the chain receives an initial data bit DDI.

All the test control inputs TE receive a signal CB from the control means or control circuit MCD. When the signal CB takes the value 0, for example, it constitutes a first control signal and a data bit at the input D of a flip-flop is then delivered to the output SO on the next rising edge of the clock CK. On the other hand, when the signal CB takes the value 1, it constitutes a second control signal and, in this case, each flip-flop delivers the data bit at the test input TI to the output SO in time with the rising edges of the clock signal CK.

A comparator or comparator means are further provided, here in the form of a EXCLUSIVE NOR logic gate PL2. A first input of the logic gate PL2 is connected to the test output SO of the flip-flip BC0 at the end of the chain. The other input of the logic gate PL2 receives the expected data bits DAi sequentially. The output of the logic gate PL2 is a logic signal that takes the value 0 or 1 in time with the comparison operations and as a function of their result.

A counter CT, incremented in time with the clock signal CK, counts from 0 to n - 1. Assuming that the value 0 is representative of the rank of the test bit DT0, the least significant bit of the value of the counter is equal to 0 for the test bit DT0, 1 for the test bit DT1, and 0 for the test bit DT2. Logically combining the least significant bit LSB (ai) of the read address and the least significant bit LSB

(rgi) of the counter value in the EXCLUSIVE NOR logic gate PL1 supplies sequentially the values 1, 0 and 1 corresponding to the test word at the address a0 in the memory plane PMM. If the test word stored at the address a0 had been 0 1 0, the logic gate PL1 would simply have been an EXCLUSIVE OR gate.

Independent Claim 9

The invention of independent Claim 9 is directed to a method of testing a sequential access memory plane PMM to store p words each made up of n bits (e.g. page 5, lines 12-19). In the method, p test words each made up of n test bits DT are written in the memory array (e.g. page 5, line 36 through page 6, line 3, and page 8, line 20 through page 9, line 33). The p test words are sequentially extracted from the memory plane and the n test bits of the extracted words are compared with expected binary data bits DAi, so that for each test word extracted, the corresponding test bits are compared sequentially with n respective expected data bits before extracting the next test word (e.g. page 6, line 12 through page 7, line 27).

Independent Claim 11

The invention of independent Claim 11 is directed to a method of testing a sequential access memory plane PMM to store words each made up of bits (e.g. page 5, lines 12-19). In the method, test words each made up of test bits DT are written in the memory array (e.g. page 5, line 36 through page 6, line 3, and page 8, line 20 through page 9, line 33). The test words are sequentially extracted from the memory plane and the test bits of the extracted words are compared with expected binary data bits DAi, so that for each test word extracted, the corresponding test bits are compared sequentially with respective expected data bits before

extracting the next test word (e.g. page 6, line 12 through page 7, line 27).

Independent Claim 14

Independent Claim 14 is directed to a sequential access semiconductor memory device including a memory array PMM for storing p words each made up of n bits (e.g. page 5, lines 12-19), and test logic connected to the memory array. The test logic includes a first test means MT1, MUXi, MUXB for writing p test words each having n test bits in the array PMM (e.g. page 5, line 36 through page 6, line 3, and page 8, line 20 through page 9, line 33), and a second test means BC0-BC2, MCD, PL2 (e.g. page 6, line 12 through page 7, line 27 of the specification and FIG. 1) for sequentially extracting the p test words from the memory array and, for each extracted test word, sequentially comparing the corresponding n test bits with expected data bits, before extracting the next test word.

Independent Claim 20

Independent Claim 20 is directed to a sequential access semiconductor memory device including a memory array PMM (e.g. page 5, lines 12-19), and test logic connected to the memory array. The test logic includes a first test circuit (e.g. MT1, MUXi, MUXB) for writing test words each having test bits in the array PMM (e.g. page 5, line 36 through page 6, line 3, and page 8, line 20 through page 9, line 33), and a second test circuit (e.g. BC0-BC2, MCD, PL2) for sequentially extracting the test words from the memory array and, for each extracted test word, sequentially comparing the corresponding test bits with expected data bits, before extracting the next test word (e.g. page 6, line 12 through page 7, line 27 of the specification and FIG. 1).

Independent Claim 26

Independent Claim 26 is directed to a test circuit for a sequential access semiconductor memory device having a memory array PMM (e.g. page 5, lines 12-19). The test circuit includes a first test circuit (e.g. MT1, MUXi, MUXB) for writing test words each having a plurality of test bits in the array (e.g. page 5, line 36 through page 6, line 3, and page 8, line 20 through page 9, line 33), and a second test circuit (e.g. BC0-BC2, MCD, PL2) for sequentially extracting the test words from the memory array and, for each extracted test word, sequentially comparing the corresponding test bits with expected data bits, before extracting the next test word(page 6, line 12 through page 7, line 27 of the specification and FIG. 1).

B. Conclusion

Appellants believe that the above Summary of the Claimed Subject Matter meets the requirements of 37 C.F.R. 41.37(c)(1)(v). The above represents a concise explanation of the subject matter defined in each of the independent claims involved in the appeal, referring to the specification by page and line number, and to the drawing Figs. 1 and 2, by reference characters; and identifies the structure, material, or acts described in the specification as corresponding to each claimed function for every means plus function for each independent claim involved in the appeal by reference to the specification by page and line number, and to the drawings by reference characters, as required by 37 CFR 41.37(c)(1)(v).

Accordingly, Appellants request that such Summary of the Claimed Subject Matter be entered and considered by the Board of Patent Appeals and Interferences. It is submitted that all of the claims are patentable over the prior art. Again, the Board of Patent Appeals and Interferences is

respectfully requested to reverse the earlier unfavorable decision by the Examiner.

Respectfully submitted,

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